applying said second periodic signal received at said second input terminal to a control electrode of said transistor of the or each even amplifier stage, to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases; and

(iv) an output terminal connected to the output of said last amplifier stage for outputting a generated frequency divided signal;

wherein said first and second generating means are arranged to generate the respective first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistances.

REMARKS

Claims 31-58 have been cancelled without prejudice, and new claims 59-84 have been added. Claims 59-84 are now pending.

Respectfully submitted,

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